REMARKS

Claims 1-2, 4-22, 33-34, and 36-60 are currently pending in the Application. Claims 1, 9, 33, 41, and 55 are currently amended, without acquiescence in the cited basis for rejection or prejudice to pursue the original claims in a related application. Applicants submit that the deleted claim elements are not needed for forming the basis for the arguments or for clarifying the claimed inventions as embodied in the respective claims. The Specification is currently amended to correct the use of a punctuation. No new matter has been added.

I.   Claim Rejections Under 35 U.S.C. §112, First Paragraph

Claims 9-22 and 41-54 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to complying with the written description requirement. Applicants respectfully traverse.

A.   For claims 9 and 41:

According to the Office action, the subject matter of the claimed limitation of "annotating the software simulation model with performance information of a hardware together with which the software simulation model runs" of claims 9 and 41 was allegedly not described in the specification in violation of the written description requirement. Applicants respectfully disagree.

Applicants respectfully submit that 35 U.S.C. § 112, first paragraph, only requires that the claimed invention as a whole be adequately **described in the specification**, MPEP § 2161, and that "there is **no in haec verba requirement**" MPEP § 2163. That is, "[t]he subject matter of the claim **need not be described literally** (i.e., **using the same terms or in haec verba**) . . . ." MPEP § 2163.02 (emphasis added.)

Applicants respectfully point to some exemplary paragraphs in the Specification which provide clear support for the claimed limitations. Applicants further respectfully note that these exemplary paragraphs are provided below for illustration and ease of explanation purposes. For example, Applicants respectfully point to ¶ [0014] which explicitly states "the simulation model is annotated with statically estimated performance information based on

the architecture of the hardware the production software executable will run on." Applicants further point to ¶ [0015] which further states that "the simulation model is annotated with formulas for dynamically determining performance information based on the architecture of the hardware the production software executable will run on". Applicants respectfully submit that these two paragraphs along provide clear support for the aforementioned claimed limitations and satisfy the requirement under 35 U.S.C. § 112, first paragraph. Applicants thus respectfully request withdrawal of the rejections and reconsideration of claims 9, 41, and their respective dependent claims.

II.   Claim Rejections-35 U.S.C. §103

Claims 1-2, 4-13, 15-19, 21-22, 33-34, 36-45, 47-51, 53-55, 57-58, and 60 stand rejected under 35 U.S.C. §103(a) as unpatentable over Passerone, *"Fast Hardware/Software Co-Simulation for Virtual Prototyping and Trade-Off Analysis"*, 1997, Proceedings of Design Automation Conference 1997 (hereinafter Passerone) in view of U.S. Patent No. 6,230,114 issued to Hellestrand (hereinafter Hellestrand) further in view of Zivojnovic, *Compiled HW/SW Co-simulation, 1996* (hereinafter Zivojnovic). Applicants respectfully traverse.

A.   Without acquiescence in the cited basis for rejection or prejudice to pursue the original claims in a related application, the currently amended claim 1 recites at least the following limitations. Claims 9, 33, 41, and 55 also recite similar limitations.

> generating a software simulation model by translating the assembler code or disassembling a binary code into a high level language format and by annotating the software simulation model with information related to estimation or determination of the performance of hardware on which the software program runs to capture a dynamic interaction between tasks during runtime, wherein **the act of annotating the software simulation model is performed during a time when the act of generating a software simulation model by translating the assembler code or disassembling a binary code;**

(emphasis added.)

According to the Office action, Passerone does not disclose or suggest the above claimed limitation but Hellestrand and Zivojnovic do. Applicants respectfully agree that

Passerone does not disclose the aforementioned limitations but respectfully disagree that Hellestrand and Zivojnovic do.

A.   The Office action cites to various items in Fig. 3A of Hellestarnd and purports that Fig. 3A and the corresponding text disclose the aforementioned limitation of "generating a software simulation model using the assembler code". Applicants respectfully disagree.

Applicants respectfully submit that **none of claims 1, 9, 33, 41, and 55 recite the limitation** of "generating a software simulation model using the assembler code" as provided in the Office action. Rather, claim 1 recited "generating a software simulation model by disassembling the assembler code into a high level language format . . .". Therefore, Applicants respectfully submit that the basis for rejection of the aforementioned limitation based upon Fig. 3A of Hellestrand is improper and respectfully request withdrawal of the rejections and reconsideration of these claims.

B.   The Office action admits that Passerone does not disclose the limitation containing the term "disassembling". Applicants respectfully agree that Passerone does not disclose, teach, or suggest at least the "disassembling" limitation of these claims. Applicants further respectfully submit that Zivojnovic does not disclose, teach, or suggest the claimed limitation of "generating a software simulation model . . . by disassembling a binary code into a high level language format . . ." of claims 1, 9, 33, 41, and 55.

According to the Office action, § IV of Zivojnovic discloses the above claimed limitations. Applicants respectfully submit that § IV of Zivojnovic remains absolutely silent on the aforementioned limitation and thus may not be used to preclude the patentability of claims 1, 9, 33, 41, 55, and their respective dependent claims under 35 U.S.C. § 103(a).

C.   Applicants respectfully submit that the current amendment to claims 1, 9, 33, 41, and 55 renders the rejection moot. Applicants further respectfully submit that Passerone teaches away from the aforementioned limitation and thus may not be used to prevent ability of these claims under 35 U.S.C. § 103(c).

Applicants respectfully submit that MPEP 2144.05 mandates that "[a] prima facie case of obviousness may also be rebutted by showing that the art, in any material respect,

teaches away from the claimed invention." MPEP 2144.05(III), citing In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

To the extent that the Office action considers Passerone's timing annotated C code as disclosing the claimed limitation of "by annotating the software simulation model with information related to estimation or determination of the performance of hardware", which Applicants strenuously disagree, Applicants respectfully submit that Passerone does not disclose, teach, or suggest the above limitation.

In § 2.2 as relied upon by the Office action, Passerone explicitly states that "[t]he formal specification of the system to be modeled is **first translated** by POLIS into a network of CFSMs, and **then synthesized as timing annotated C code** as described above." ¶ 1, § 2.2, left hand column (emphasis added.) That is, in Passerone's approach, the timing annotated C code is generated during the synthesis stage from **a network of CFSMs** rather than based at least in part upon "**the assembler code**" which "is an assembly-language representation of the software representation. Therefore, Applicants respectfully submit that Passerone does not disclose, teach, or suggest at least the aforementioned claimed limitation and thus may not be used to preclude the patentability of claims 1, 9, 11, 33, 41, and 55 under 35 U.S.C. § 103(a) for at least the foregoing reasons.

D.   For claim 55:

Claim 55 recites at least the following limitations.

> parsing the assembly language software module **into a data structure**, the data structure comprising one or more **nodes**, each of the one or more nodes being **mapped to a period of time** using a **mapping definition**, each of the one or more nodes **containing an element of the assembly language software module**;

(emphasis added.)

According to the Office action, Passerone does not disclose the above limitation but items 313 and 315 of Fig. 3A in Hellestrand do. Applicants respectfully agree that Passerone does not disclose the above limitation but respectfully disagree that Hellestrand does.

Item 313 in Fig. 3A of Hellestrand "includes parsing assembly language of file 311 line by line to determine the time delay in clock cycles required for each line, and the size in

bytes of target code of each line",. col. 22, ll. 28-30, and that "[t]he result of the assembly parsing the timing analysis step 313 is a set of timings for each linear block in the 'C' code." Col. 22, 37-38. Moreover, 315 of Fig. 3A shows "[t]he timing and size information of the blocks". Col. 22, ll. 39-41. Nonetheless, Applicants respectfully submit that this disclosure of Hellestarnd fails to disclose at least the claimed limitations of "parsing . . . into a data structure" which comprises "one or more nodes", "mapping definition", "each of the one or more nodes containing an element of the assembly language software module" of claim 55, much less the claimed limitation as recited above in block quote.

As such, Applicants respectfully submit that claim 55 is believed to be allowable over Passerone, Hellestrand, and Zivojnovic for at least the above additional reasons.

III.   Claim Rejections-35 U.S.C. §103

Claims 14 and 46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Passerone as modified by Hellestrand and Zivojnovic in view of Hartoog et al, *Generation of Software Tools from Processor Descriptions for Hardware / Software Codesign*, Proceedings of the 34th Design Automation Conference, June 9-13, 1997 (hereinafter Hartoog). Applicants respectfully traverse.

As the final Office Action does not rely on Hartoog in forming the basis for rejection of the limitation in section IV-A, Applicants respectfully submit that claims 14 and 46 are believed to be allowable over Passerone, Hellestrand, Zivojnovic, Hartoog, and their combination for at least the foregoing reasons as presented in section IV-A above and their dependency on claim 1 and 41.

IV.   Claim Rejections-35 U.S.C. §103

Claims 20, 52, and 59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Passerone as modified by Hellestrand and Zivojnovic further in view of Suzuki et al, *Efficient Software Performance Estimation Methods for Hardware/Software Codesign*, 1996 Proceedings of the 33rd Annual Conference on Design Automation (hereinafter Suzuki). Applicants respectfully traverse.

As the final Office Action does not rely on <u>Suzuki</u> in forming the basis for rejection of the limitation in section IV-A, Applicants respectfully submit that claims 20, 52, and 59 are believed to be allowable over <u>Passerone</u>, <u>Hellestrand</u>, <u>Zivojnovic</u>, <u>Suzuki</u>, and their combination for at least the foregoing reasons as presented in section IV-A above and their dependency on claim 1 and 41.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

Applicant(s) hereby explicitly retracts and rescinds any and all of the arguments and disclaimers presented to distinguish the prior art of record during the prosecution of all parent and related application(s)/patent(s), and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Vista IP Law Group's Deposit Account No. **50-1105**, referencing billing number **7012162001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Vista IP Law Group's Deposit Account No. **50-1105**, referencing billing number **7012162001**.

Respectfully submitted,

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